

CALL FOR PAPERS
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY
Special Section on Efficient HEVC Implementations

High Efficiency Video Coding (HEVC) is the newest compression standard, developed by the ITU-T | ISO/IEC Joint Collaborative Team on Video Coding (JCT-VC), which consists of experts from the ITU-T's Visual Coding Experts Group (VCEG) and ISO/IEC's Moving Picture Experts Group (MPEG). Its first version has been approved by the standardization organizations in Spring 2013. The HEVC design represents the standardization community's new best algorithms for video coding in terms of coding efficiency. To achieve this, algorithmic features have been included in HEVC that are substantial advances over those in previous standards. However, some of these new features that were standardized have been shown to provide higher coding efficiency only at an increase of encoder or decoder complexity or both. Hence, the real-time implementation of HEVC encoders and decoders is a challenging task that the video coding community is actively working on. This special section has been created to cover the area of efficient design of HEVC implementations for both encoders and decoders in hardware as well as software.

Potential topics of interest include, but are not limited to:

- **Implementation-friendly encoding algorithms** that efficiently trade off coding efficiency and complexity
- **Efficient-VLSI hardware** for HEVC encoders or decoders, with focus on reducing power consumption and efficient-area/memory utilization; applications of low power design techniques are of particular interest
- **High-throughput VLSI hardware** for HEVC encoders or decoders, with focus on reaching resolutions and frame-rate up to Ultra-HD 8k @ 120fps
- **High-throughput software implementations** on multi-core processors, DSP, and GPU
- **Ultra-low latency implementations** of HEVC for interactive applications such as video conferencing
- **Parallel-processing in implementations** to leverage the built-in parallelism features of HEVC
- **Caching architectures** for reducing memory bandwidth for HEVC
- **SW/HW partitioning for HEVC**
- **FPGA implementations** of HEVC encoders or decoders, with a focus on high-throughput and low efficient-resource utilization

Important Dates

Initial Paper Submission:	November 14, 2014
Initial Paper Decision:	January 1, 2015
Revised Paper Submission:	February 1, 2015
Revised Paper Decision:	April 1, 2015
Final Paper Submission:	May 1, 2015
Final Paper Decision:	June 1, 2015
Publication Date:	September 2015

Manuscript submissions and reviewing process

Submission of a paper to CSVT is permitted only if the paper has not been submitted, accepted, published, or copyrighted in another journal. Papers that have been published in conference and workshop

proceedings may be submitted for consideration to CSVT provided that (i) the authors cite their earlier work; (ii) the papers are not identical; and (iii) the journal publication includes novel elements (*e.g.*, more comprehensive experiments). For submission information, please consult the IEEE CSVT Information for Authors: <http://tcsvt.polito.it/authors.html>.

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